A modeling framework for safe code on (Multi-Core) Controllers

INTRODUCTION





M.Sc. Thomas Barth



Prof. Dr. -Ing. Peter Fromm

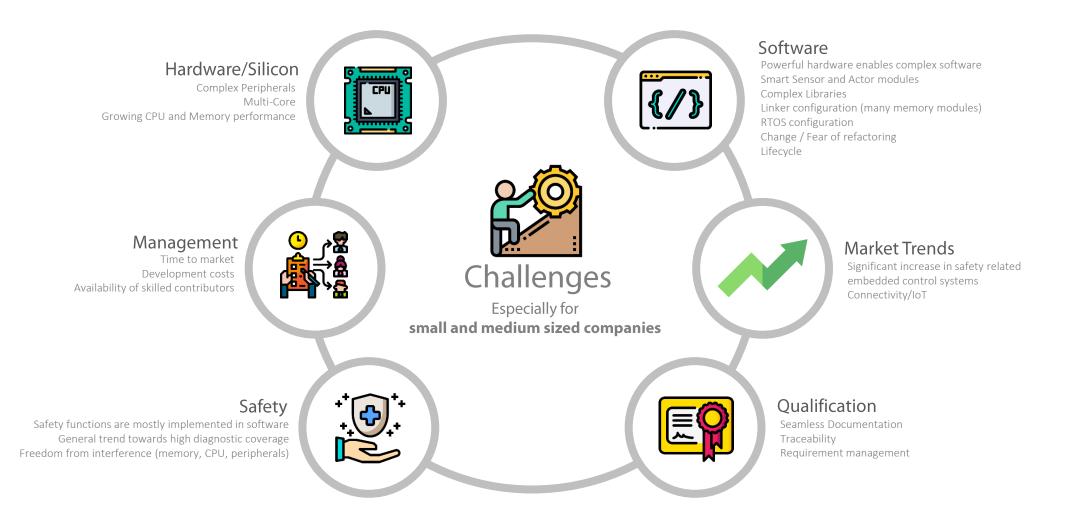


h_da



μRTE Introduction

Motivation



Project timeline



Initial idea

Prof. Fromm starts the implementation of a lightweight runtime environment to be used in the academic environment



First industrial contact

Prof. Fromm consults the company Linde who considers to introduce AUTOSAR[™] on an AURIX[™] multi-core microcontroller for forklift control. After an evaluation phase, an improved version of the lightweight runtime environment is introduced instead.

Thomas Barth joins the research group for his master thesis and starts a PhD program afterwards.

Concept phase



Public funding

Along with the FZI at the Karlsruhe Institute of Technology and the company HighTec, the research group at Hochschule Darmstadt attracts funding for 2 years to research the applicability of multi-core microcontrollers for safety critical applications.

A feasibility study is conducted in which an possible framework for product development is identified. The development of µRTE starts during this phase.



Industrial evaluation

An prototype of µRTE is evaluated in an industrial project in which the software for an safety relevant HMI for an agricultural machine is implemented.

In this project, µRTE is used for software architecture definition, code generation, requirement management and documentation generation.

2021



Pre-Release

A first version of µRTE including all core-features is released:

- Software Modeling
- Hardware Modeling
- Functional Modeling
- Requirements Modeling

2022

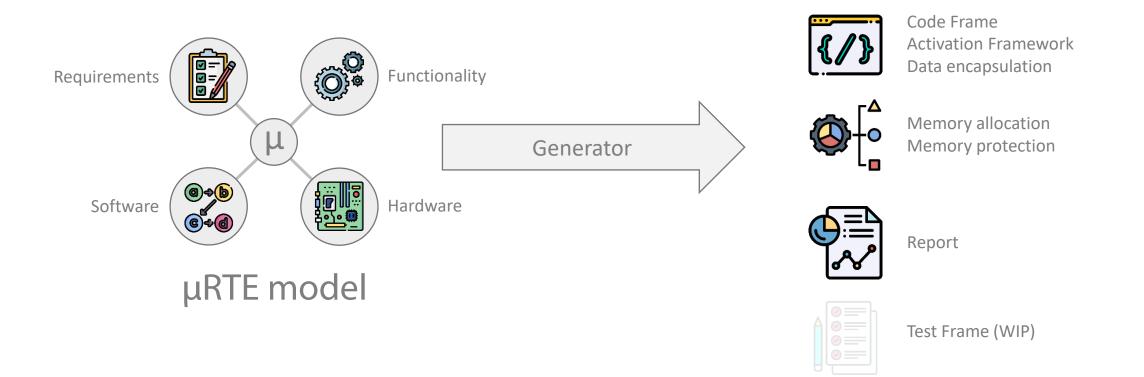
- Automated model assessment
- Code generation
- Report generation

2010 > 2013 > 2014 > 2015 > 2016 >2017 2018 > 2019 >2011 2012

2020





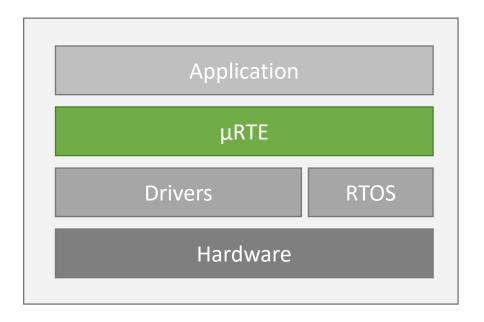


Features



Portability

- Any RTOS
- Any Controller Single/Multi-Core
- Any Toolchain (C/C++ on GCC implemented)





Software features

- Cyclic and Signal driven activation of runnables
- Multiple system-states with own data-flows
- Extensive system and application error handling
- Human readable code



Safety

- Complete modeling of the safety case
- Inbuilt consistency and safety checks
- Complete traceability from requirements to implementation units
- Supports freedom from interference
- Generated code complies with MISRA standard

Process

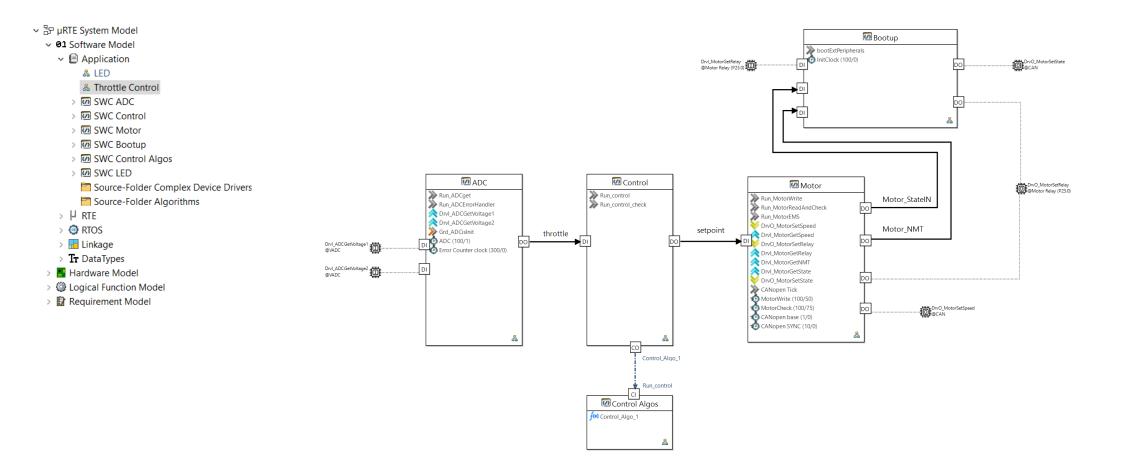
- Encourages clean and modular solutions
- Eclipse plugin implementation
- Intuitive and rich graphical modeling
- Complete support of V-model
- Extensive auto-generated documentation

Software modeling

Each block represents a code file in which software functions are contained

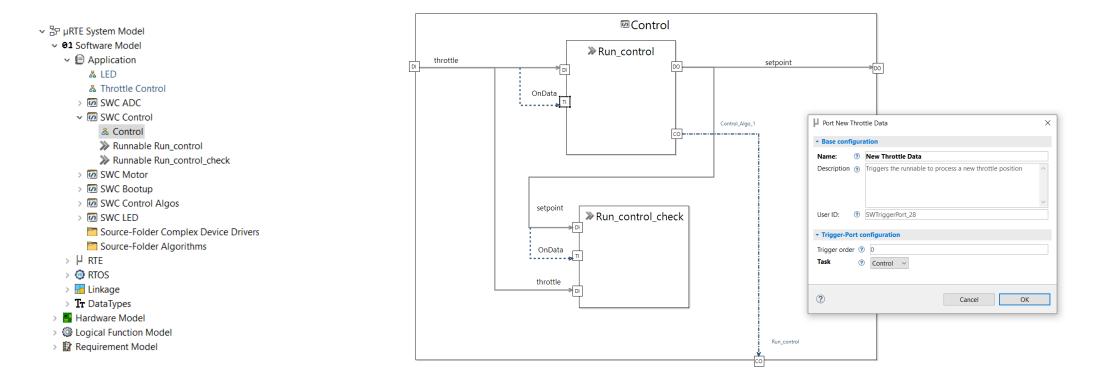
Arrows represent data exchange

Chip-lcons represent hardware interfaces



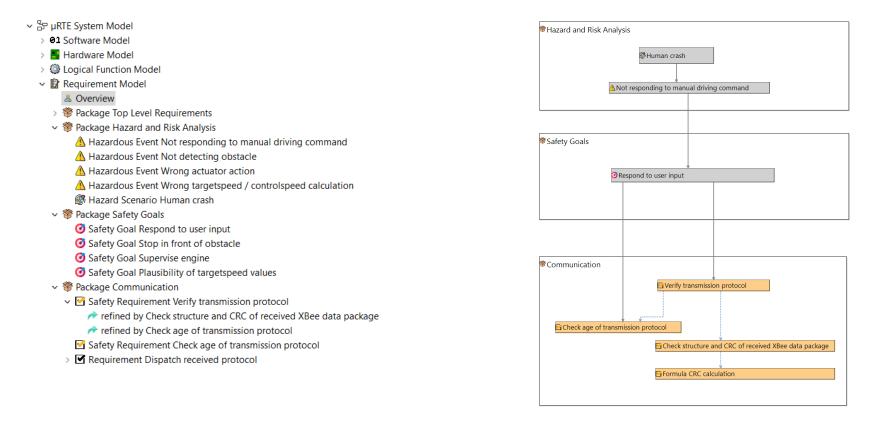
Software modeling

Detailed view describes runnable execution



Requirements modeling

Derivation of requirements Relationship (refinement/conflict) among requirements Mapping to implementation units



Report

Generated as HTML Each object in the model has a an own report page Properties and dependencies are shown textual and graphical

uRTE	Car_5 Runnable ENGINE_setSpeed_run (Ri	unnable_125)		Search
PL Software Model E Software	≫ Runnable			
+ 🐼 SWC BSW CanOpen	ENGINE_setSpeed_	run		
+ 60 SUC_Control - 20 SUC_CON	Calculate the speed for the 4 engines			
	Warnings			- 0
	Safety (1) Safety Warnings for this Runnable. Safety warnings are related to the Require	ements Layer, especially the SIL		
+ W SWC_drive_1_pong Complex Device Drives + V are + Ganglex Device Drives + Units - Units - Units - Tr Destigoe	 Design (3) Design Warnings for this Runnable Design warnings are related the configuration 	ation of elements within the model.		
Hardware Model	Diagrams			
C Tegurenet Model				
	Logical Function Model	Requirements Model	01 Software Model	Hardware Model
	Safety			
		Req	uired	
	SIL derived			SIL_1
	overwrite (SIL_manual)			derived
	reason (SIL_manual_reason)			
	SIL			SIL_1
		Ach	ieved	
	SIL achieved			QM
	justification			

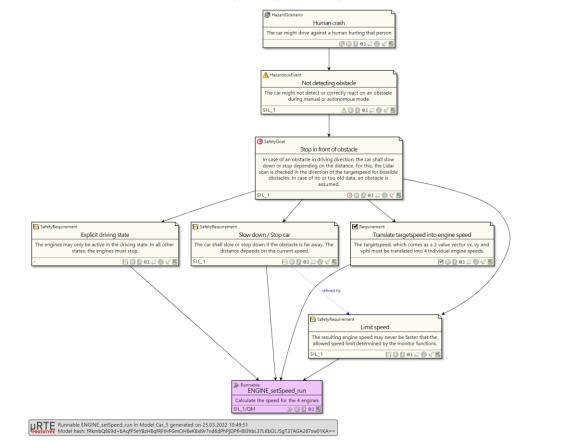
lequirement Layer				
✓ (Safety)Requirements (4) (Safety)Requirements referencing to runnable ENGINE_setSpeed_r	un.			
oftware Layer				
➡ IN Signals (2) Ingoing signals of runnable ENGINE_setSpeed_run.				
OUT Signals (1) Outgoing signals of runnable ENGINE_setSpeed_run. Hidden columns: * Tasks = SystemStates = Requirements = miminum Age = maximu > Datatype (D) = Alt-In (D) = Alt-Out (D) = In-Driver (D) = Out-Drive				value (D) » Pointer access (D)
Signal 🔺 🛡	Type ▲▼ X	Storage AV X	Runnables OUT	Runnables IN AV X
FAULHABER_speed_out Interface towards the speed object on the motion controller	Data	local in BaseSystem	>>> ENGINE_setSpeed_run	≫ CANOPEN_tx_run
max Tasks (1) Tasks runnable ENGINE_setSpeed_run is executed by.				
Activation-Events (1) Activation Events triggering the execution of runnable ENGINE_se	tSpeed_run.			
Runnables providing data (2) Runnables providing data for runnable ENGINE_setSpeed_run.				
Runnables triggered (1) Runnables triggered by runnable ENGINE_setSpeed_run.				
Runnables receiving data (1) Runnables receiving data from runnable ENGINE_setSpeed_run.				
lardware Layer				
Hardware Components (1) Hardware runnable ENGINE_setSpeed_run is associated with. Inclu signals.	iding executing CPUs,	hardware referenced	by its protectionSets and driver	a to a connecting

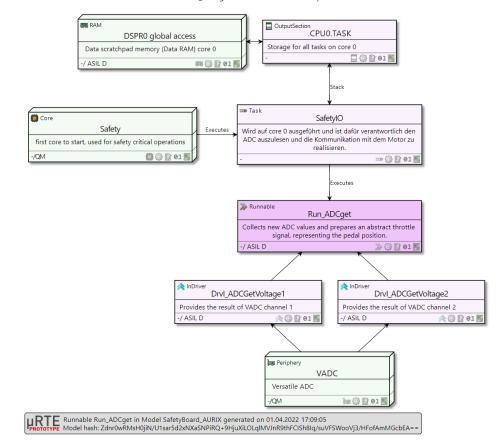
µRTE Introduction

Report

Generated as HTML Each object in the tree has a an own report Properties and dependencies are shown textual and graphical

Runnable ENGINE_setSpeed_run - Requirements Model Dependencies





Runnable Run_ADCget - Hardware Model Dependencies

Report

Checkers for inconsistency, safety and design Warnings are reported as globally and associated with affected elements

Aonitor_cyclicCheck_run	
as runnable will perform cyclic sanity checks for the system	
Varnings	-
Safety (2) Safety Warnings for this Runnable. Safety warnings are related to the Requirements Layer, especially the SIL	
>>> Monitor_cyclicCheck_run has a SIL effective of SIL_1 but a SIL achieved of QM	
Multiple Technical functions for ≫ Monitor_cyclicCheck_rum 🧐 Data transmission over XBee, 🧐 Detect obstacle	

) errors, 76 warnings, 0 others	
Description	Location
 	
6 Core Arm Cortex®-M7 (QM) was selected for execution for ActivationEngine which does not satisfy the SIL required of SIL_1.	ActivationEngine
OyclicEvent CAN_dispatch_clock is not associated with any trigger port.	CyclicEvent_CAN_dispatch_clock
DataType bool is unused.	DataType_bool
DataType CAN_RX_MSG_t is unused.	DataType_CAN_RX_MSG_t
a DataType int16_t is unused.	DataType_int16_t
DataType sint32_t is unused.	DataType_sint32_t
a DataType uint32_t is unused.	DataType_uint32_t
a ECU PSOC SmartPower has a SIL effective of SIL_1 but a SIL achieved of QM	ECU_PSOC SmartPower
Intersection DRIVE 0 calibration fun is not directly associated with a Technical Function.	Function DRIVE 0 calibration fun

Safety Warnings (2)	
II Safety Warnings of this model. afety warnings are related to the Requirements Layer, especially the SIL.	
.CPU0.TASK is set as stack for task 🐲 Safety/O but has more references: 🛠 ActivationEngine, 🐲 Safety/O.	
.CPU0.TASK is set as stack for the central activation engine but but has more references: 父 ActivationEngine, 🛥 Safety	ylO.
🔊 Design Warnings (3)	
All Design Warnings of this model. Design warnings are related the configuration of elements within the model.	
The Runnable Data-Port-IN name "setpoint" was given multiple times at runnables: » Run_MotorWrite, » Run_control_ch	heck
The Runnable Data-Port-IN name "throttle" was given multiple times at runnables: 🐎 Run_control, 🐎 Run_control_check	
StatchPool does not contain any signals.	
	(B) (B) (A) (A)
WatchPool does not contain any signals. RTE Warnings (6) All RTE Warnings of this model. RTE warnings are related to the configured behaviour of the RTE.	(B) (B) (1) (A)
RTE Warnings (6) All RTE Warnings of this model.	(iii)
RTE Warnings (6) All RTE Warnings of this model. RTE warnings are related to the configured behaviour of the RTE.	
 RTE Warnings (6) All RTE Warnings of this model. RTE warnings are related to the configured behaviour of the RTE. <i>LEDs</i> has no maximum age and therefore never expires. 	
 RTE Warnings (6) All RTE Warnings of this model. RTE warnings are related to the configured behaviour of the RTE. <i>LEDs</i> has no maximum age and therefore never expires. <i>Motor_SpeedOUT</i> has no maximum age and therefore never expires. 	It is the responsibility of the user to make
 RTE Warnings (6) All RTE Warnings of this model. RTE warnings are related to the configured behaviour of the RTE. <i>LEDs</i> has no maximum age and therefore never expires. <i>Motor_SpeedOUT</i> has no maximum age and therefore never expires. <i>Motor_StateOUT</i> has no maximum age and therefore never expires. Local signal buffers for runnables will be created without initial value and the invalid signal behavior is set to "no update". 	It is the responsibility of the user to make

Code

Runnables and other functions (Drivers etc.): Developer works in designated code blocks Documentation and dependencies are generated as comment

/* Runnable "ENGINE setSpeed run"	* SAFETY
* Calculate the speed for the 4 engines	* SIL manual: derived
*	* SIL effective: SIL 1
	* SILachieved: 0M
* User-ID: Runnable_125	Sit achieved: On
* SystemStates: "normal"	
* WCET: 0	* Requirements
* Stack: 0	 "Translate targetspeed into engine speed"
* ROM: 0	* Description:
* *	
	The targetspeed, which comes as a 3 value vector vx, vy and vphi must be translated into 4 individual engine speeds.
* Triggers	
* - TriggerPort "TI_ENGINE_setSpeed_run_50_0ms"	* SafetyRequirements
* Task: "Safety"	 "Explicit driving state" SIL effective: derived
* System Events:	* Description:
 Cyclic Trigger "setSpeedClock" Cycle Time: 50, Offset 0 	
ž	* The engines may only be active in the driving state. In all other states, the engines must stop.
* Data Signals IN	* Other References of the SafetyRequirement:
	 Runnable Monitor cyclicCheck run
 BataPort "DI_CONTROL_limits" User-ID: SWDataPort_129 	* - "Limit speed" SIL effective: SIL 1
* Signals:	
* - "CONTROL_limits" User-ID: SignalDataObject_14:	* Description:
* Description: Structure containing driving limiting parameters like maxSpeed	* The resulting engine speed may never be faster that the allowed speed limit determined by the monitor functions.
* Age: Max: 300	* - "Slow down / Stop car" SIL effective: SIL 1
* Storage: Signalpool "Safety"	* Description:
 Payload Datatype: generated, see #CONTROL limits_cfg.h 	
	* The car shall slow or stop down if the obstacle is far away. The distance depends on the current speed.
 <u>Runnables</u> writing to this signal: 	* Other References of the SafetyRequirement:
* - SWC "SWC_Monitor"	* - Runnable Monitor cyclicCheck run
* - "Monitor_cyclicCheck_run"	
*	
 DataPort "DI CONTROL targetspeed" User-ID: SWDataPort 126 	
* Signals:	* Start of user code ENGINE_setSpeed_run implementation notes
* - "CONTROL targetspeed" User-ID: SignalDataObject 16:	#
	* End of user code
* Description: The car targetspeed	*/
* Age: Max: 300	
* Storage: local signal	#void ENGINE_setSpeed_run(
* Payload Datatype: generated, see #CONTROL targetspeed_cfg.h	
* Runnables writing to this signal:	/* Trigger */
* - SWC "SWC Control"	const uRTE Triggers t triggerPort,
* - "CONTROL drive run"	
- CONTROL_01176_roll	
	/* Incoming Data-Signals */
* Data Signals OUT	Signal_CONTROL_limits& sig_IN_CONTROL_limits, /* Structure containing driving limiting parameters like maxSpeed */
 * - DataPort "D0_FAULHABER_speed_out" User-ID: SWDataPort_128 	Signal CONTROL_targetspeed& sig_IN_CONTROL_targetspeed, /* The car targetspeed */
* Signals:	
* - "FAULHABER_speed_out" User-ID: SignalDataObject_20:	/# Onterior Data Circula #/
* Description: Interface towards the speed object on the motion controller	/* Outgoing Data-Signals */
* Storage: local signal	Signal_FAULHABER_speed_out* const p_sig_OUT_FAULHABER_speed_out /* Interface towards the speed object on the motion controller */
){
Payload Datatype: generated, see #FAULHABER_speed_out_cfg.h	
 <u>Runnables</u> reading from this signal: 	//local IN signal value buffers
* - SWC "SWC_BSW_CanOpen"	
* - "CANOPEN_tx_run"	Signal_CONTROL_limits::data_t CONTROL_limits_data;
 Trigger: 	Signal_CONTROL_targetspeed::data_t CONTROL_targetspeed_data;
* OnData:	5 MM M M M M M M M M M M M M M M M M M
 "TI CANOPEN tx run FAULHABER speed out onData" triggering runnable "CANOPEN tx run" in Task "Safety" 	//Start of user code implementation ENGINE_setSpeed_run
* - ITCHMOLEM_CV_LOU_HACK_Sheed_onf_Unback_CLABBeLTUB LOUMADAGE CHMOLEM_CX_LOU_TU_HASK_SALE()	There is a more substance and semication enoting seconderal on

Code

Internal code: Focus on readability and simplicity Generic and minimalistic low level interfaces for easy integration Avoidance of inheritance with dedicated code generated for each element

uRTE_boolean_t Signal_ADC1::isValid(void) const {

//return value buffer
uRTE_boolean_t ret = false;

//check if signal is in the valid state
ret = uRTE_SignalStatus_valid==this->m_content.m_status;

//check age only if previous steps succeeded
if(uRTE_true==ret){

```
//signal age buffer
const uRTE_SignalTime_t signal_age = uRTE_getTimeStamp() - this->m_content.m_timestamp;
```

//check if the signal is older than the maximal age
if(SIGNAL_ADC1_AGE_MAX<signal_age){</pre>

```
//signal is too old
ret=uRTE_false;
```

```
}
```

```
//check checksum only if previous steps succeeded
if(uRTE_true==ret){
    ret = uRTE_checkChecksum(&(this->m_content), sizeof(Signal_ADC1::content_t), this->m_checksum);
}
return ret;
```

```
}
```

Signal internal code

static const PxProtectRegion_T Task_Control_Regions[] = {

```
//RTE
uRTE_TAE_CONTROL_MEMPROTSET
```

```
//do not remove this line!
{0,0,(PxProtectType_t)0}
```

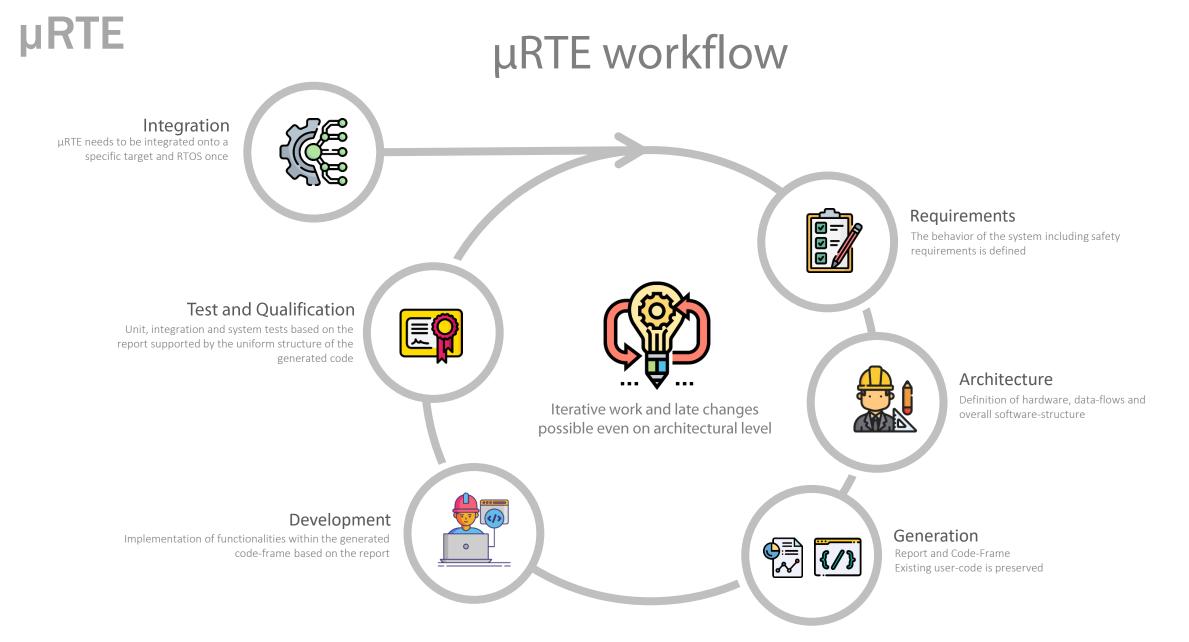
};

void CTask_Control::Task_Func(PxTask_t myID, PxMbx_t myMailbox, PxEvents_t myActivationEvents)
{
 //Run activation engine

```
uRTE_TAE_Control::Run();
```

Task integration

μRTE Introduction



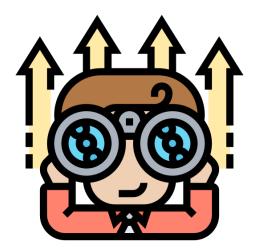
Experience



 μRTE Demonstrator

- Fast familiarization
- Code focus moves to architectural focus
- Significantly improved system understanding
- Architectural refactoring support
- Cross platform reusability
- Good code analyzability / debugability

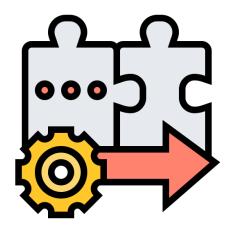
Possible extensions



- Test-Framework generation (WIP)
- OS-less implementation
- Extension towards interrupts, centralized error handling and more
- Certifiable implementation
- Readback of generated artifacts and comparison against model
- Linkage to other tools, CI/CD etc.

Integration

Interfaces



- One additional system task with central tick
- Tasks are not generated
- Global timestamp source
- Interfaces for inter-task messaging and notification